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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/316,560	05/24/1999	MARC DURANTON	PHF-99.540V	7958

7590 12/18/2002

c/o U.S. PHILIPS CORPORATION
INTELLECTUAL PROPERTY DEPARTMENT
580 WHITE PLAINS ROAD
TARRYTOWN, NY 10591

EXAMINER
BRAGDON, REGINALD GLENWOOD

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/316,560	Applicant(s) DURANTON, MARC	
	Examiner Reginald G. Bragdon	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 03 October 2002 .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-5 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. The request for a continued prosecution application (CPA) under 37 CFR 1.53(d) filed on 03 October 2002 is acknowledged. 37 CFR 1.53(d)(1) was amended to provide that the prior application of a CPA must be: (1) a utility or plant application that was filed under 35 U.S.C. 111(a) before May 29, 2000, (2) a design application, or (3) the national stage of an international application that was filed under 35 U.S.C. 363 before May 29, 2000. *See Changes to Application Examination and Provisional Application Practice*, interim rule, 65 *Fed. Reg.* 14865, 14872 (Mar. 20, 2000), 1233 *Off. Gas. Pat. Office* 47, 52 (Apr. 11, 2000). Since a CPA of this application is not permitted under 37 CFR 1.53(d)(1), the improper request for a CPA is being treated as a request for continued examination of this application under 37 CFR 1.114. *See id.* at 14866, 1233 *Off. Gas. Pat. Office* at 48.

Remarks

2. It is noted that on 11 October 2002 the Office mailed a "Notice of Improper CPA filing under 37 CFR 1.53(d)" along with a "Notice of Improper Request for Continued Examination (RCE)". In response thereto, Applicant filed a Notice of Appeal on 17 October 2002. However, the "Notice of Improper Request for Continued Examination (RCE)" was mailed only to indicate that the request for a continued prosecution application ("CPA") under 37 CFR 1.53(d) was being treated as a request for an RCE. Applicant's Notice of Appeal is not required in order to extend the time for response to the final office action of 17 July 2002 since the Application is

currently in status as an RCE awaiting a first office action. Furthermore, the Notice of Appeal has not been entered since there was no outstanding Office Action awaiting response in the application at the time the Notice of Appeal was filed. It is noted however that the Applicant's deposit account (#14-1270) was charged the Notice of Appeal fee of $320 on 24 October 2002.

Claim Objections

3. Claims 1-3 are objected to because of the following informalities:

In claim 1, line 6, "independent" should be deleted.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Torii et al. (4,734,850).

As per claims 1, 4, and 5, Torii et al. teaches a data processing system including a plurality of execution units (E-units 1 and 6 in figure 1), which represent a "first processor" and a "second processor". A "memory system" is shown in figure 2, including memory banks 47, 48

("plurality of memory circuits"), which are independent of each other. See column 2, line 67, to column 3, line 1. These FIFO memories of figure 2 are shared between and accessible by the execution units as described in column 2, lines 7-15. A mode indicating circuit 41 ("master controller") provides a signal for repetitively indicating at a constant interval a write mode to banks 47, 48. See column 3, lines 26-43. A read/write control circuit 100 ("control unit") generates a write address from a write control circuit 42 for write data (see column 4, line 60, to column 5, line 22) and a read address from read control circuit 43 for read data (see column 6, line 64 to column 7, line 11). Furthermore, Torii et al. teaches writing to one bank 47 simultaneously with reading from the other bank 48, and visa versa. See column 7, lines 46-52.

Torii et al. ensures that a particular bank is not simultaneously required for reading and writing through the use of a write enable input. If the write enable input is "1", then data is written into a particular bank. See column 6, lines 21-28. Since the bank is enabled for writing through the write enable input, it would be impossible to simultaneously read from the same bank (which would require a write enable input of "0"), thereby ensuring that input data and output data are not simultaneously required for writing and reading from one of the memory banks. The input to each bank's write enable input is generated by the read/write control circuit 100. See figure 2.

As per claim 2, Torii et al. teaches a write counter and a read counter for generating addresses. See claim 18, for example, and figures 4 and 5.

As per claim 3, Torii et al. teaches a write request input, WREQ, ("NXT_W") and a read request input, RREQ, ("NXT_R"). See column 4, lines 2-13, and column 6, lines 39-41.

Response to Arguments

6. Applicant's arguments filed 03 October 2002 have been fully considered but they are not persuasive.

Applicant argues on page 4 of the response that as "shown in Fig. 1 [of Torii et al.],...only one respective E-unit (4-6) is capable of accessing any one of the FIFO memory units". However, element 1 of figure 1 is also an E-unit. Therefore, FIFO memory 22 is coupled to and accessible by E-unit 6 and E-unit 1. This is described at column 2, lines 7-15, as set forth in the rejection.

Applicant also argues that Fig. 7 of Torii et al. teaches that "the FIFO memories are allocated to input or output ports using the distribution logic circuit...and are not all accessible by the E-units". However, Fig. 7 is an embodiment of Torii et al. that is not relied upon to teach the claimed invention. The elements of Applicant's invention are taught by the embodiment of Torii et al. set forth in figures 1 and 2.

Applicant argues on pages 4-5 that Torii et al. does not teach "a control unit for, on the basis of control commands, ensuring that input data and output data are not simultaneously required for writing and reading from one of the plurality of memory circuits and where the each of the plurality of memory circuits is accessible by a first and a second processor." However, Torii et al. teaches a read/write circuit 100 in figure 2 which represents a "control unit". A write control circuit 42 of the read/write circuit 100 uses an address generated for write data (see column 4, line 60, to column 5, line 22) and a read address from read control circuit 43 for read data (see column 6, line 64 to column 7, line 11). Furthermore, Torii et al. teaches writing to one bank 47 simultaneously with reading from the other bank 48, and visa versa. See column 7, lines

46-52. Torii et al. ensures that a particular bank is not simultaneously required for reading and writing through the use of a write enable input. If the write enable input is "1", then data is written into a particular bank. See column 6, lines 21-28. Since the bank is enabled for writing through the write enable input, it would be impossible to simultaneously read from the same bank (which would require a write enable input of "0"), thereby ensuring that input data and output data are not simultaneously required for writing and reading from one of the memory banks. The input to each bank's write enable input is generated by the read/write control circuit 100. See figure 2. As discussed above, the memory circuit (i.e. memory banks 47, 48 in figure 2) of each FIFO memory (e.g. FIFO memory 22) is accessible by E-unit 6 and E-unit 1.

On page 5 of the response, Applicant states that "it is noted that Torii et al. specifically teaches that a 'selected FIFO memory performs read and write operations concurrently and intermittently'". However, it is not clear how this teaches away from ensuring that input data and output data are not simultaneously required for writing and reading from the same memory as detailed in the rejection of the claims.

Conclusion

7. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)

or

(703) 746-7239 (Official Communications)

(703) 746-7240 (For Status inquiries, draft communications)
and/or
(703) 746-5693 (Use this FAX#, only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal page/amendment be faxed directly to them on occasion).

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
December 16, 2002